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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,866	09/11/2003	Honorio T. Granada	018865-004410US	8678
20350	7590 02/10/2005		EXAM	INER
	D AND TOWNSENI	OWENS, DO	OWENS, DOUGLAS W	
EIGHTH FLO	RCADERO CENTER OOR		ART UNIT	PAPER NUMBER
SAN FRANC	CISCO, CA 94111-383	34	2811	

DATE MAILED: 02/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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	Application No.	Applicant(s)			
	10/660,866	GRANADA ET AL.			
Office Action Summary	Examiner	Art Unit			
	Douglas W. Owens	2811			
The MAILING DATE of this communication appeariod for Reply	opears on the cover sheet with the	correspondence address			
A SHORTENED STATUTORY PERIOD FOR REP THE MAILING DATE OF THIS COMMUNICATION - Extensions of time may be available under the provisions of 37 CFR 1 after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a re - If NO period for reply is specified above, the maximum statutory perio Failure to reply within the set or extended period for reply will, by statu- Any reply received by the Office later than three months after the mail earned patent term adjustment. See 37 CFR 1.704(b).		mely filed ys will be considered timely. n the mailing date of this communication. ED (35 U.S.C. § 133).			
Status					
1) Responsive to communication(s) filed on					
	is action is non-final.				
	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.				
Disposition of Claims		•			
4) ☐ Claim(s) 9-16 is/are pending in the application 4a) Of the above claim(s) is/are withdress 5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) 9-16 is/are rejected. 7) ☐ Claim(s) is/are objected to. 8) ☐ Claim(s) are subject to restriction and/ Application Papers	awn from consideration. for election requirement.				
9) The specification is objected to by the Examiner.					
10)⊠ The drawing(s) filed on 19 November 2004 is/are: a)⊠ accepted or b) objected to by the Examiner.					
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).					
11) The oath or declaration is objected to by the E	•				
Priority under 35 U.S.C. § 119					
12) Acknowledgment is made of a claim for foreig a) All b) Some * c) None of: 1. Certified copies of the priority documer 2. Certified copies of the priority documer 3. Copies of the certified copies of the pri application from the International Bure: * See the attached detailed Office action for a list	nts have been received. nts have been received in Applicat ority documents have been receiv au (PCT Rule 17.2(a)).	ion No ed in this National Stage			
Attachment(s)					
Notice of References Cited (PTO-892) Notice of Draftsperson's Patent Drawing Review (PTO-948)	4) Interview Summan Paper No(s)/Mail D				
 Notice of Dialisperson's Falent Diawing Review (F10-940) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08 Paper No(s)/Mail Date 12/19/03; 11/19/04. 		Patent Application (PTO-152)			

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 2. Claims 9, 10 and 12 14 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,629,835 to Mahulikar et al.

Regarding claim 1, Mahulikar et al. teach a method of making a chip device (Fig. 13, for example), comprising:

providing a die (54);

providing a leadframe (62) including a die attach cavity and a plurality of dimples defined around a periphery of the leadframe (Col. 7, lines 34 – 39), the die attach cavity having substantially the same thickness as the die;

placing solder balls into the dimples; and

flipping the die into the die attach cavity and attaching it therein.

Regarding claim 10, Mahulikar et al. teach a method, wherein the die provided is a bumped die.

Regarding claim 12, Mahulikar et al. teach a method, further comprising placing solder (70) on the die.

Regarding claim 13, Mahulikar et al. teach a method, wherein the leadframe comprises a copper based alloy (Col. 7, lines 11 – 16).

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Regarding claim 14, Mahulikar et al. teach a method, wherein the leadframe includes a solderable coating (64).

Claim Rejections - 35 USC § 103

- 3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 4. Claims 11 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mahulikar et al. as applied to claim 9 above, and further in view of US Patent No. 6,627,991 to Joshi.

Regarding claim 11, Mahulikar et al. do not teach a method, wherein the die comprises a MOSFET. Joshi teaches a method of making a chip device, wherein the die comprises a MOSFET (Fig. 8; Col. 5, lines 20 – 53, for example). It would have been obvious to one having ordinary skill in the art at the time of the invention to incorporate the teaching of Joshi into the method taught by Mahulikar et al., since the chip and chip device are ideally suited for a MOSFET, or power MOSFET. Furthermore, chip commonly include MOSFETs for use in memory and logic devices for example.

Regarding claim 15, Mahulikar et al. do not teach a method, wherein the die comprises source and gate connections. Joshi teaches a method wherein the die includes source and gate connections. It would have been obvious to one of ordinary

skill in the art to incorporate the teaching of Joshi into the method taught by Mahulikar et al. for reasons discussed above.

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5. Claim 16 rejected under 35 U.S.C. 103(a) as being unpatentable over Mahulikar et al. as applied to claim 1 above, and further in view of US Patent No. 6,344,687 to Huang et al.

Mahulikar et al. do not teach a method, wherein the leadframe comprises an Ni-Pd coating. Huang et al. teach a method, wherein the leadframe comprises an Ni-Pd coating (210; Col. 3, lines 31 and 32). It would have been desirable to one of ordinary skill in the art to incorporate the method taught by Huang et al. since it desirable to provide layers with high solderability.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W. Owens whose telephone number is 571-272-1662. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Douglas W Owens

Douglo V. Owen

Examiner Art Unit 2811